ispXPLD™ 5000MX Family

3.3V, 2.5V and 1.8V In-System Programmable
eXpanded Programmable Logic Device XPLD™ Family

July 2002 Advance Data Sheet

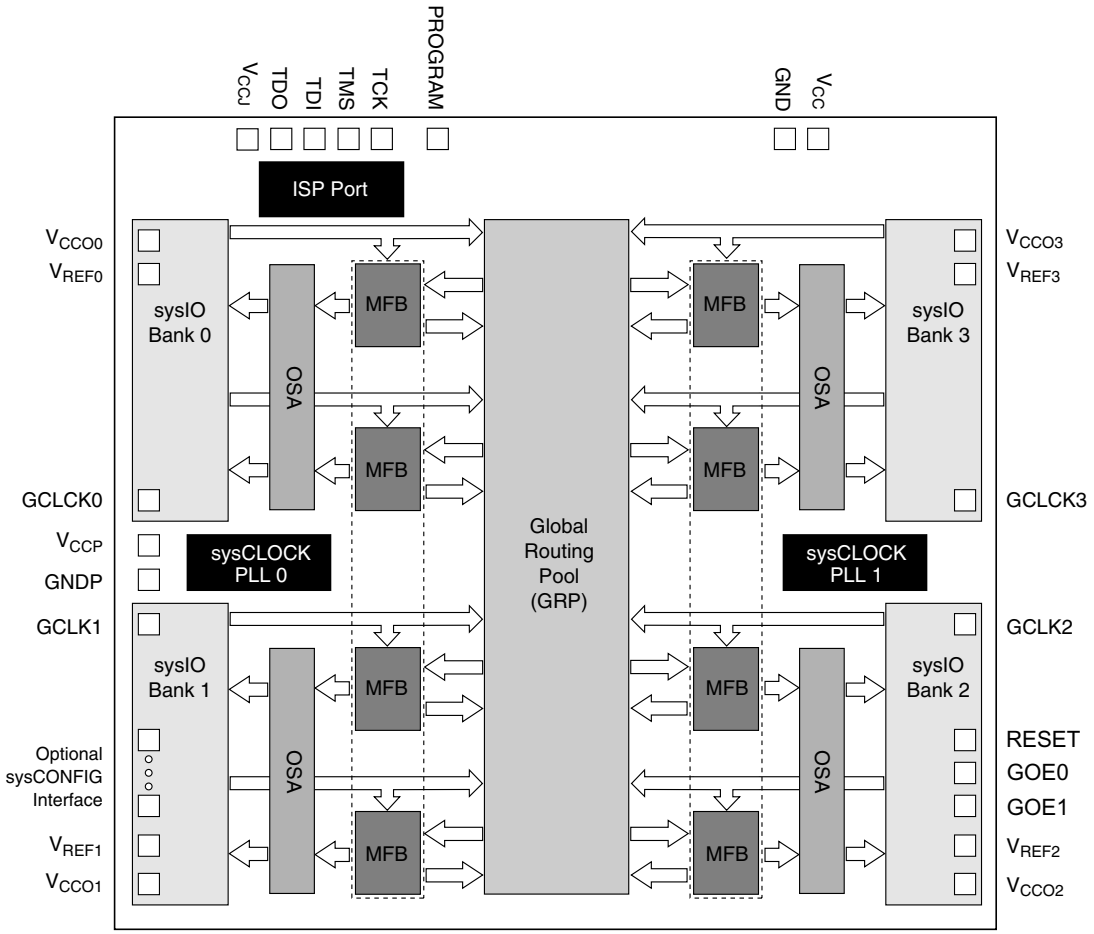
Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI-X, PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
- **Expanded In-System Programmability (ispXP™)**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ microprocessor interface
  - Design security
- **High Speed Operation**
  - 3.5ns pin-to-pin delays, 285MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Static power 20 to 50mA (1.8V) 30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and 1.8V (5000MC) power supply operation
  - IEEE 1149.1 interface for boundary scan testing
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	3.5ns	4.0ns	4.5ns	4.5ns
t_S (Register Set-up Time)	2.5ns	2.9ns	3.0ns	3.0ns
t_{CO} (Register Clock to Out Time)	2.5ns	3.0ns	3.0ns	3.0ns
f_{MAX} (Maximum Operating Frequency)	285MHz	250MHz	225MHz	225MHz
I/Os	141	149/193/253	193/317	317/381
System Gates	75K	150K	225K	300K
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programmable Logic Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 architecture by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and ternary CAM operation. In addition, sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 3.5ns, 2.5ns clock-to-out delay, 2.0ns set-up time, and operating frequency up to 285MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO interface helps users meet the challenge of today's mixed voltage designs. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD 5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Output Sharing

Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control of clock skews.

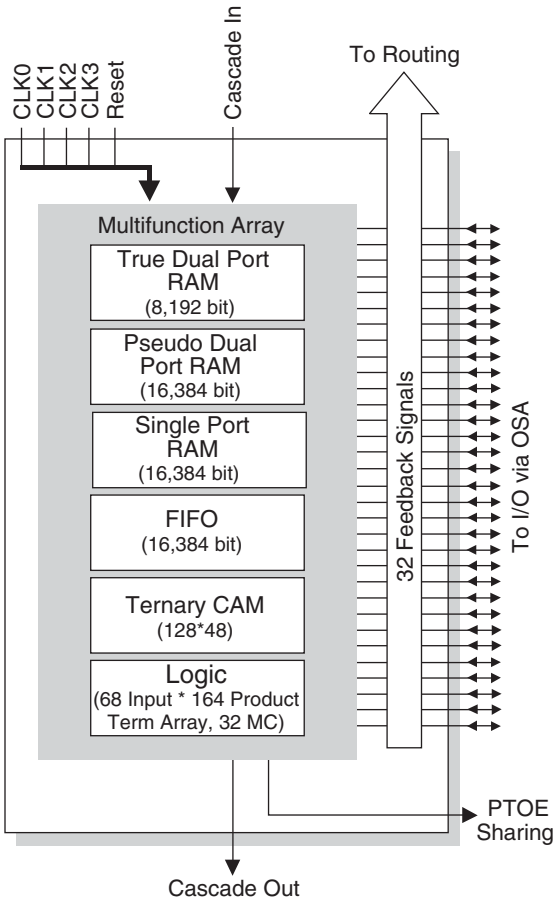
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen functions the multi-function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. The various configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram



Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details the different cascading options. There are chains of MFBs in each device which determine those MFBs that are adjacent for the purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatically cascade blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width support.

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	E → F → G → H
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z → Y
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool, which are available in both true and complement form for every product term. It is also possible to cascade adjacent MFBs to create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock enable, and output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 provides a more detailed view from the perspective of a macrocell slice.

Figure 3. MFB in SuperWIDE Logic Mode

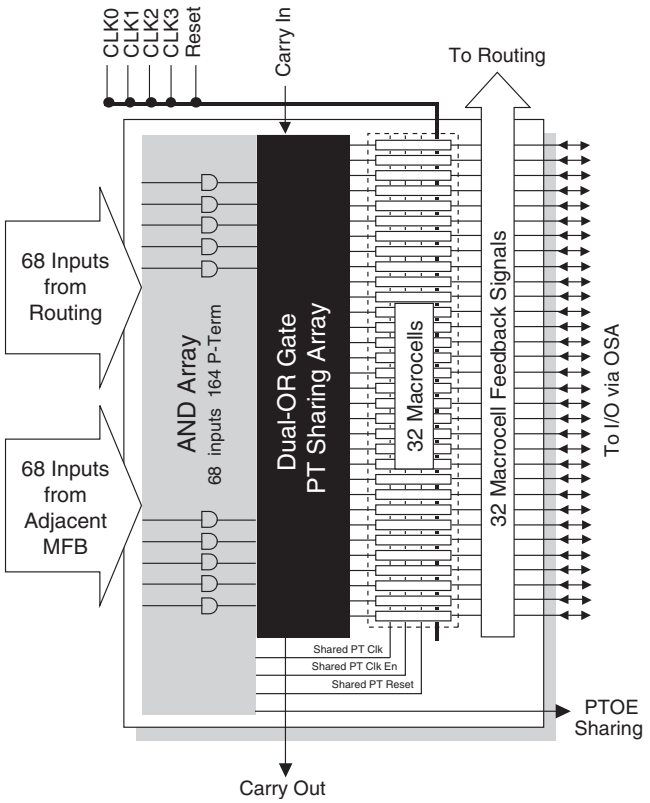
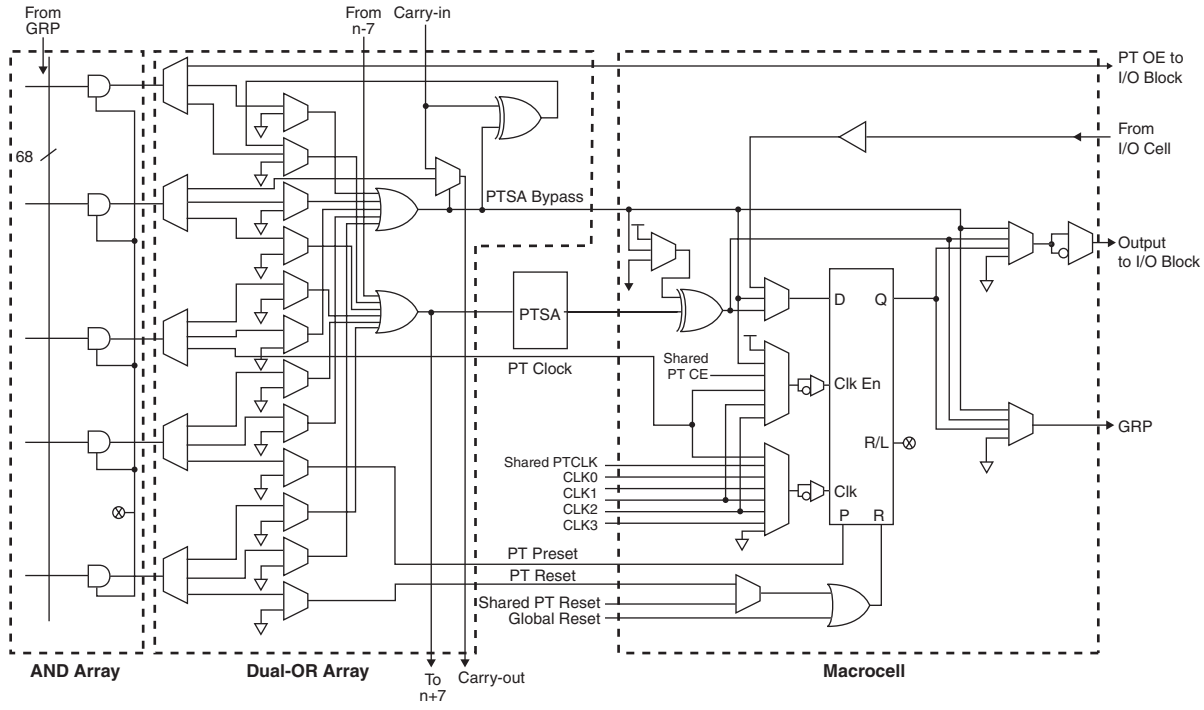


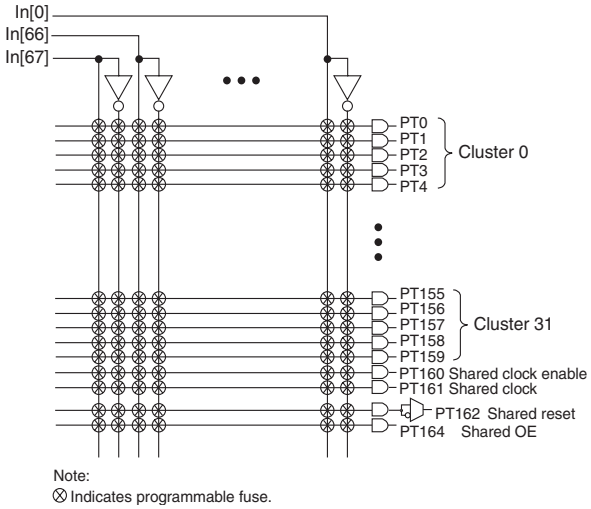
Figure 4. Macrocell Slice in Logic Mode AND-Array



AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from the GRP are used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array can be connected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms feed the Dual-OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Clock Enable, Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product term clusters. There is one product term cluster for every macrocell in the MFB. In addition to the four control product terms, the first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Preset and PT Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array

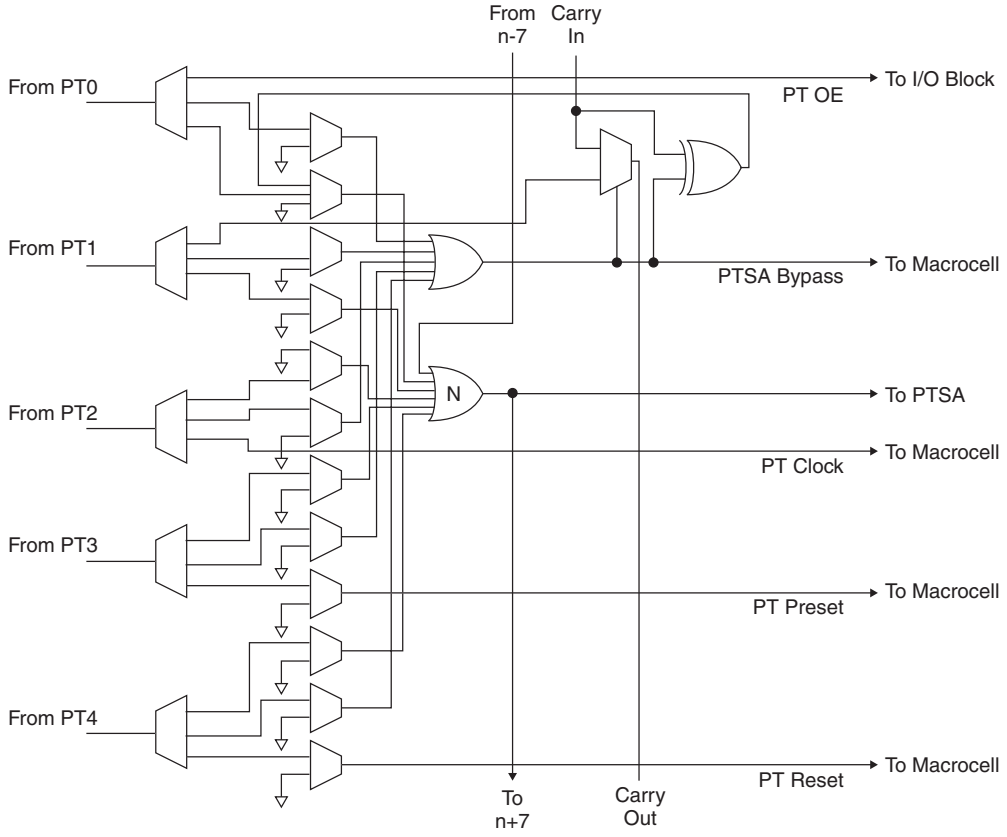


Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. These OR gates are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypass OR gate receives its five inputs from the combination of product terms associated with the product term cluster. The PTSA-Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate receives five inputs from the combination of product terms associated with the product term cluster. It also receives an additional input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocell associated with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other product terms and the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions. There is a small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR Array.

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic functions. This logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors can be implemented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 31. Macrocell zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it can be set to zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain flows is the same as that for PT cascading.

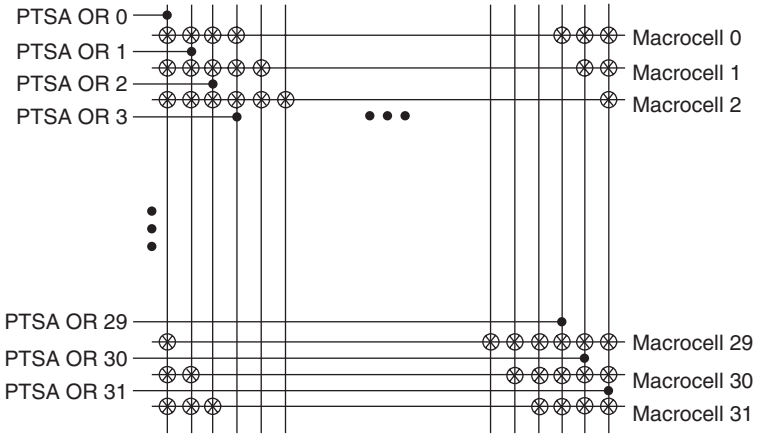
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PTSA OR) and 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven Expandable PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+1, N+2 and N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macrocell 0 gets its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allows wide functions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, the greatest number of product terms that can be included in a single function with one pass of delay is 35. Up to 160 product terms can be included in a single function through the use of the expandable PTSA OR capability. Figure 7 shows the graphical representation of the PTSA.

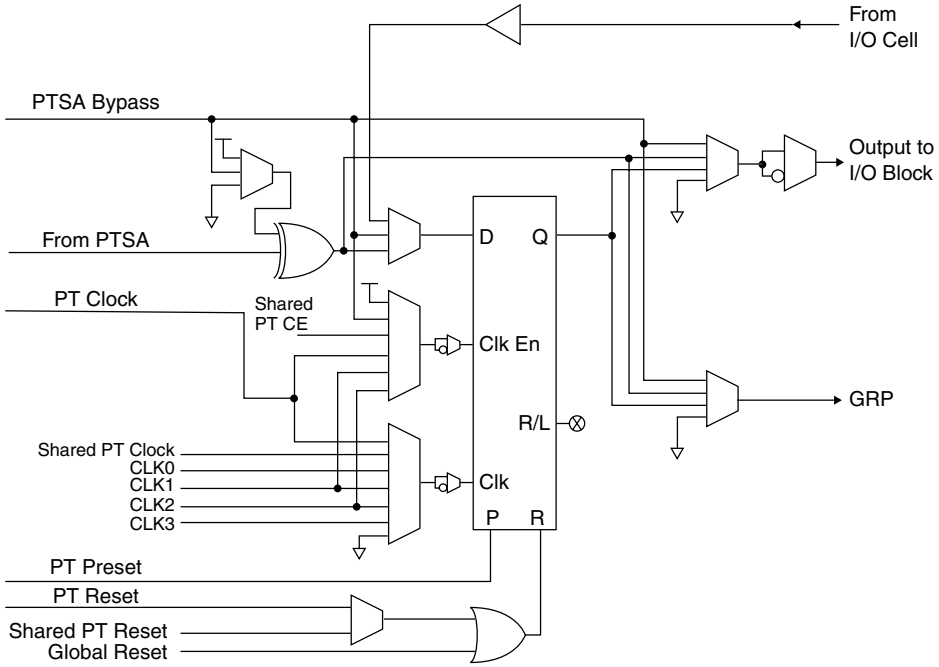
Figure 7. Product Term Sharing Array (PTSA)



Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. All macrocells have an output that feeds the GRP. Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concurrent output capability from the macrocell gives efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the macrocell.

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as detailed in Table 4. The remainder of this section details operation of each of the memory modes. Additional information regarding the memory modes can also be found in technical note number TN1030, *Using Memory in ispXPLD 5000MX Devices.*

Table 4. MFB Memory Configuration

Memory Mode	Configurations
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2048 x 8 1024 x 16 512 x 32
CAM	128 x 48

Input and Output
The data input and control signals to a MFB in memory mode are generated from inputs from the routing. Data signals are only available in the true non-inverted format. True or complemented versions of the inputs are available for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Unused inputs and outputs are not accessible in memory mode.

ROM Operation
In each of the memory modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

Increased Depth And Width
Designs that require a memory depth or width that is greater than that support by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the user's design.

Bus Size Matching
All of the memory modes apart from CAM mode support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies this mapping scheme applies to each port.

True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port share the same clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock enable, and reset selections. Selections may be made independently between both inputs and outputs and ports. Table 5 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 9. Dual-Port SRAM Block Diagram

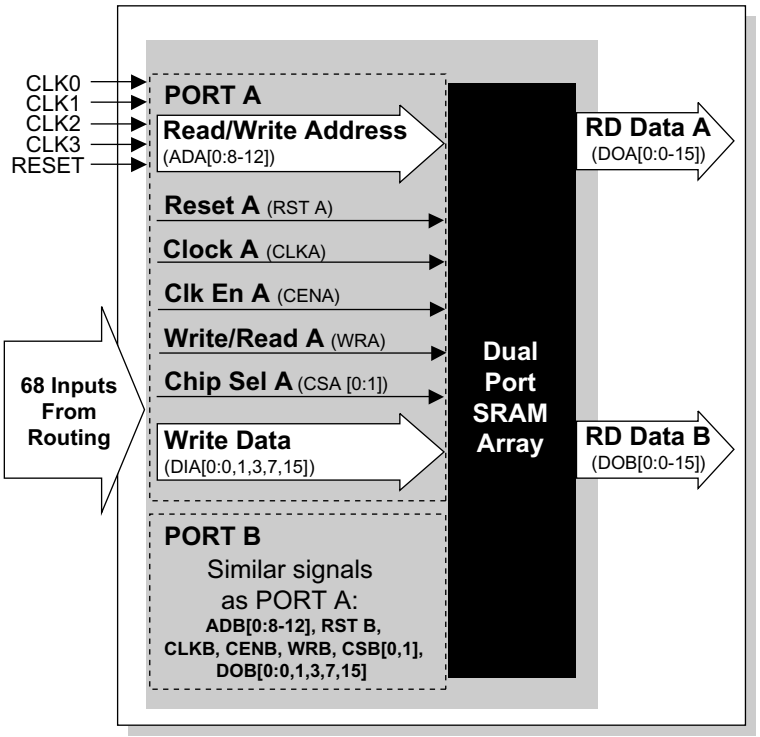


Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	Selected from CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Clock Enable	Selected from CENA (CENB) or two of the global clocks (CLK1 - CLK 2). The selected signal can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RSTA (RSTB). RSTA (RSTB) can be inverted is desired.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independent read and write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). The read data and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signals share the same clock, and clock enable. All read signals share the same clock and clock enable. Reset is shared by both read and write signals. Table 6 shows the possible sources for the clock, clock enable and initialization signals for the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

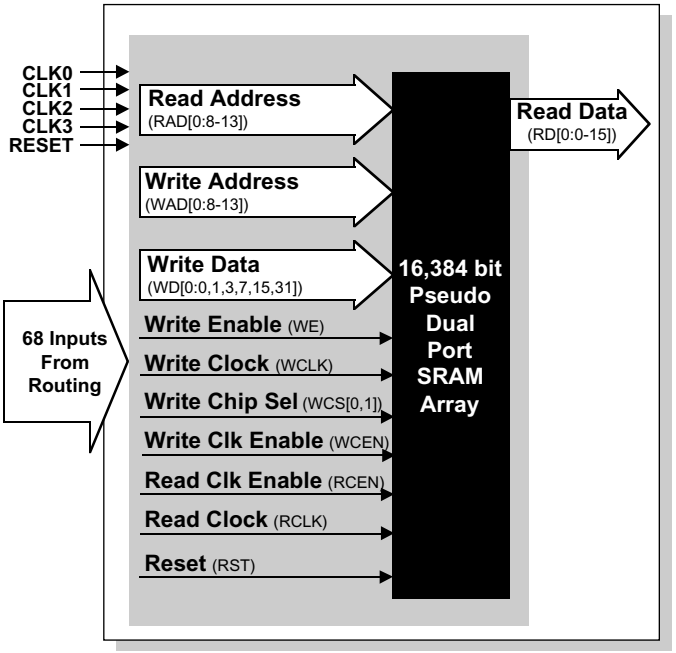


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	Selected from WCLK or one of the global clocks (CLK0 - 3). The selected signal can be inverted if desired.
	Clock Enable	Selected from WCEN or two of the global clocks (CLK0 - CLK3). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.
Read Data and Read Address	Clock	Selected from RCLK or one of the global clocks (CLK0 - 3). The selected signal can be inverted if desired.
	Clock Enable	Selected from RCEN or two of the global clocks (CLK1 - CLK2). The selected signal can be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST may have inversion if desired.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 11 shows the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common clock, clock enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

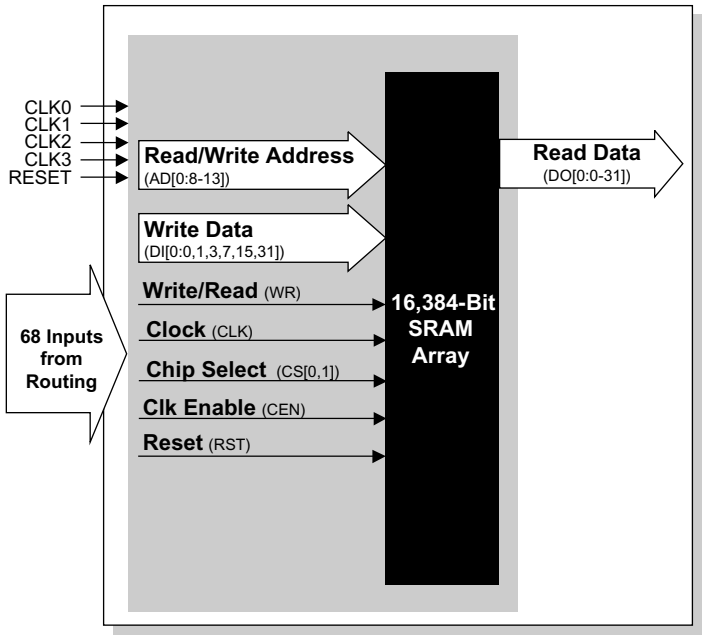


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	CEN or two of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost empty. The thresholds for Full, Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full and Full share the same clock and clock enables. Read outputs are synchronous although these can be configured in look ahead mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Reset is shared by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the various registers.

Figure 12. FIFO Block Diagram

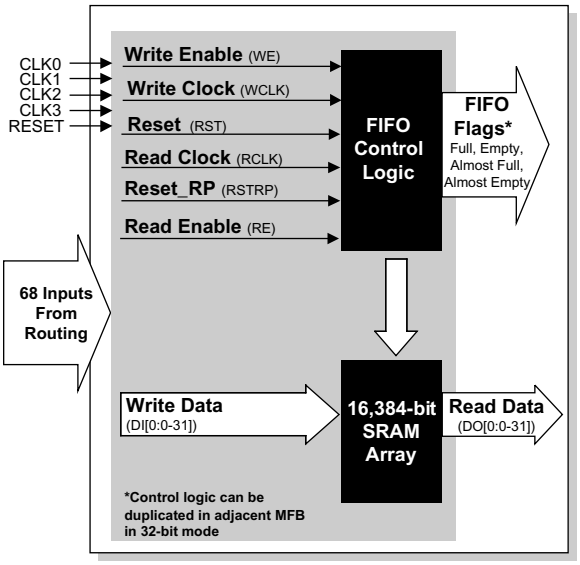


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WEN or two of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WEN or two of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	REN or two of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM). CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there is more than one match) flags are set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

The write/comp data, write address, write enable, write chip select, and write don't care signals are synchronous. The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The Enable mask register input is not latched but must meet setup and hold times relative to the write clock. All inputs must use the same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Reset is common for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and reset for the various CAM registers.

Figure 13. CAM Mode

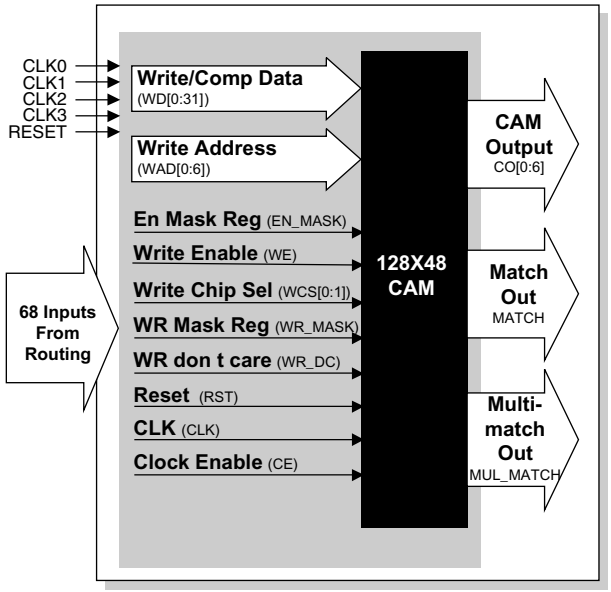


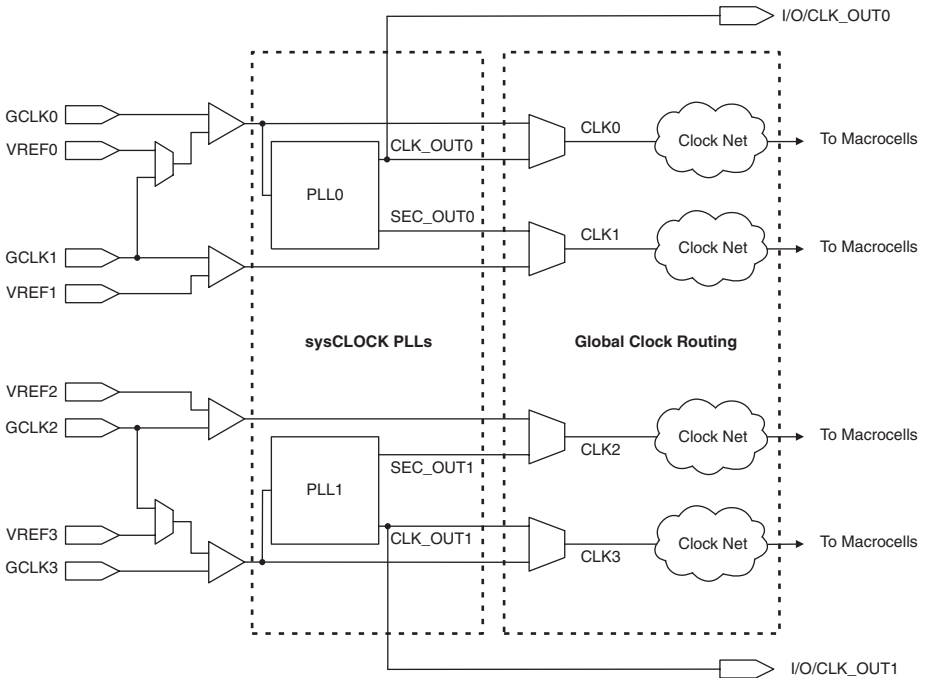
Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverted if required.
	Clock Enable	WE or two of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the multifunction array from GRP, with inversion if desired

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs. Note at each register there is the option of inverting the clock if required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are deskewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 and provides outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 and CLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from the GRP or directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows the ispXPLD 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Figure 15. PLL Block Diagram

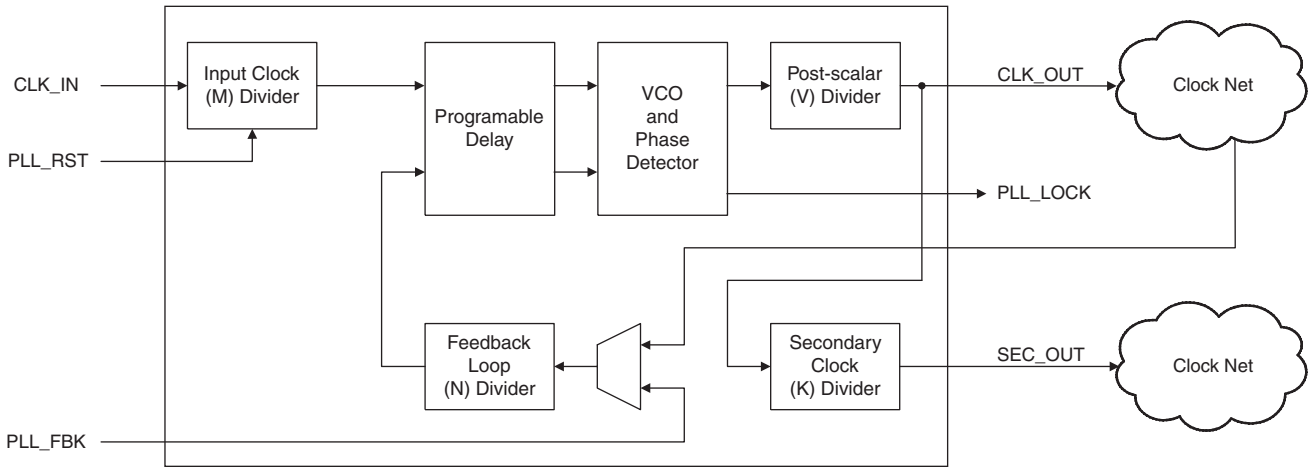
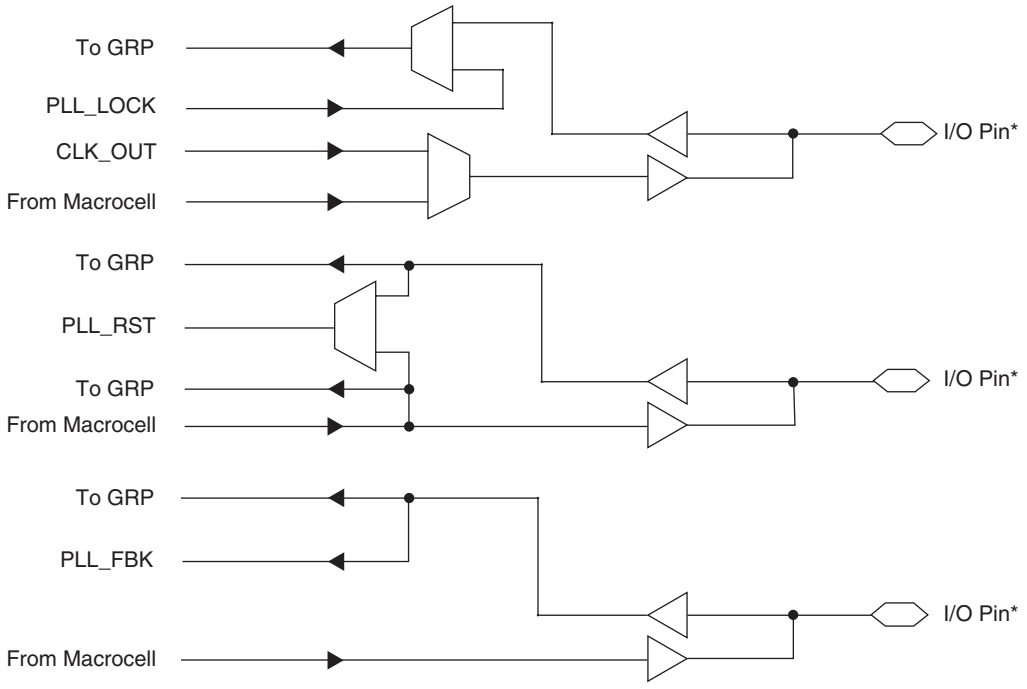


Figure 16. Connection of Optional PLL Inputs and Outputs



*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance. For more information on the PLL, please refer to Lattice technical note number TN1003, *Lattice sysCLOCK PLL Usage Guidelines.*

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedback line to its associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal per I/O cell. The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The OE MUX also has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX goes through a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The MFBs are grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PTOE signal is derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is derived from the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, every I/O cell can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

Figure 17. I/O Cell

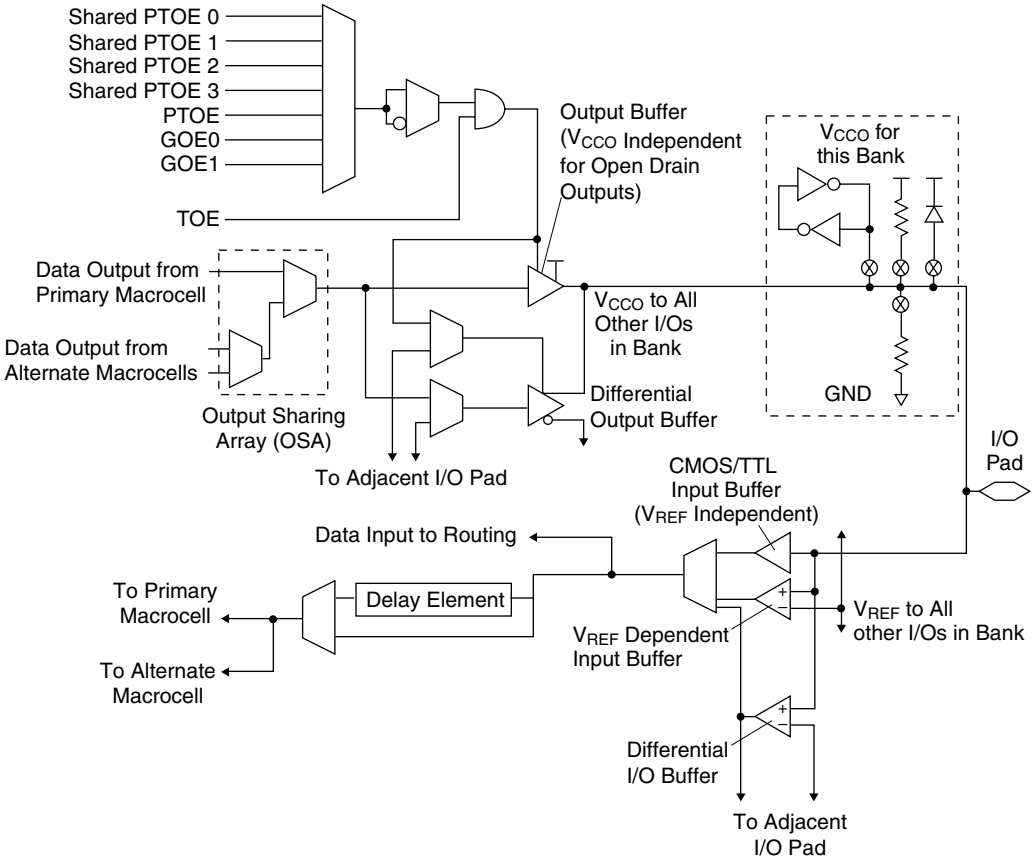


Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T))U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 11 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}. For more information on the sysIO capability, please refer to Lattice technical note number TN1000, *sysIO Design and Usage Guidelines.*

Table 11. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	N/A	N/A	N/A
PCI-X 3.3V	N/A	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75v
HSTL, Class IV	1.5V	0.9V	0.75v
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Control, Clock, and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_{REF} signal is derived from the adjacent bank. When differential standards are supported two adjacent clock pins are paired to form the input. The TOE and JTAG pins of the ispXPLD 5000MX device are the only pins that do not have sysIO capabilities. These pins only support the LVTTL and LVCMOS standards applicable to the power supply voltage of the device. The global reset global output enable pins are associated with Bank 2 and support all of the sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can

tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down device be minimal on active signals.

Programmable Drive Strength
The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programmed to a variety of different values. Thus the impedance an output driver can be closely match to the characteristic impedance of the line it is driving. This allows users to eliminate the need for external series termination resistors.

Programmable Slew Rate
The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices support two slew rates. This allows system noise and performance to be balanced in a design.

Programmable Bus-Maintenance
All general-purpose inputs have programmable bus maintenance circuitry. These are intended to maintain a valid logic level into a device when driving devices go into the tri-state mode. Four options are available for users; pull-up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device.

IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE 1532 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfiguration of the SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during the testing of a circuit board.

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor style interface (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more information on the sysCONFIG capability, please refer to technical note number TN1026, *sysCONFIG Interface Usage Guidelines.*

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit prevents readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. The security bit also prevents programming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For information on estimating power consumption, please refer to Lattice technical note number TN1031, *Power Estimation in ispXPLD 5000MX Devices.*

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os' physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family of devices allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice's ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4]	-0.5 to 4.5V	-0.5 to 4.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95	V
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7	V
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6	V
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95	V
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7	V
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6	V
T_J	Junction Temperature (Commercial Operation)	0	90	C
	Junction Temperature (Industrial Operation)	-40	105	C

E²CMOS Erase Reprogram Specifications

Parameter	Min	Max	Units
Erase/Reprogram Cycle[1]	1,000	—	Cycles

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	+/-150	µA
		V_{IH} (MAX) $\le V_{IN} \le$ 3.6V	—	—	+/-150	µA

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCO} \le V_{CCO}$ (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	10	uA
I_{PU}	I/O Active Pullup Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	30	—	150	uA
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	150	uA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	uA
I_{BHHS}	Bus Hold High sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—	uA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	uA
I_{BHLH}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	150	uA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{CCO} * 0.35	—	V_{CCO} * 0.65	uA
C1	I/O Capacitance[1]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C2	Clock Capacitance[1]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C3	Global Input Capacitance[1]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver Output Shorted	—	—	24	mA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz

Supply Current

Symbol	Parameter	Condition	Min	Typ[3]	Max	Units
ispXPLD 5512						
I_{CC}[1, 2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—		—	mA
		V_{CC} = 2.5V, f = 1.0MHz	—		—	mA
		V_{CC} = 1.8V, f = 1.0MHz	—		—	mA
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CC} = 3.3V, f = 0MHz, unloaded	—		—	mA
		V_{CC} = 2.5V, f = 0MHz, unloaded	—		—	mA
		V_{CC} = 1.8V, f = 0MHz, unloaded	—		—	mA
I_{CCOP}	PLL Power Supply Current (per PLL Bank)	V_{CC} = 3.3V, f = 10MHz	—		—	mA
		V_{CC} = 2.5V, f = 10MHz	—		—	mA
		V_{CC} = 1.8V, f = 10MHz	—		—	mA

1. Device configured with 16-bit counters.
2. ICC varies with specific device configuration and operating frequency.
3. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[2]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	—	—	—
LVCMOS 2.5	2.3	2.5	2.7	—	—	—
LVCMOS 1.8[1]	1.65	1.8	1.95	—	—	—
LVTTL	3.0	3.3	3.6	—	—	—
PCI 3.3	3.0	3.3	3.6	—	—	—
PCI-X	3.0	3.3	3.6	—	—	—
AGP-1X	3.15	3.3	3.45	—	—	—
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	—	0.9	—
HSTL Class IV	1.4	1.5	1.6	—	0.9	—
GTL+	1.4	—	3.6	0.882	1.0	1.122
LVDS[3]	2.3	2.5	3.6	—	—	—

1. Design tools default setting.
2. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported standards.

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)	I_{OH}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	2.4	20, 16, 12, 8, 5.33, 4	-20, -16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	2.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8	-8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4	-12, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
PCI -X[5]	-0.3	1.26	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36	n/a

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8
5. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} * 3.3/1.8 and V_{IH} = 0.5 * V_{CC} * 3.3/1.8

sysIO Differential DC Electrical Characteristics

Over Recommended Operating Conditions

Parameter	Description	Test Condtions	Min.	Typ.	Max.
LVDS					
V_{INP} . V_{INP}	Input Voltage		0V	—	2.4V
V_{THD}	Differential Input Threshold		+/-100mV	—	—
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05V	—	2.35V
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50mV
V_{OS}	Output Voltage Offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125V	1.20V	1.375V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—	24mA

ispXPLD 5512MX External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

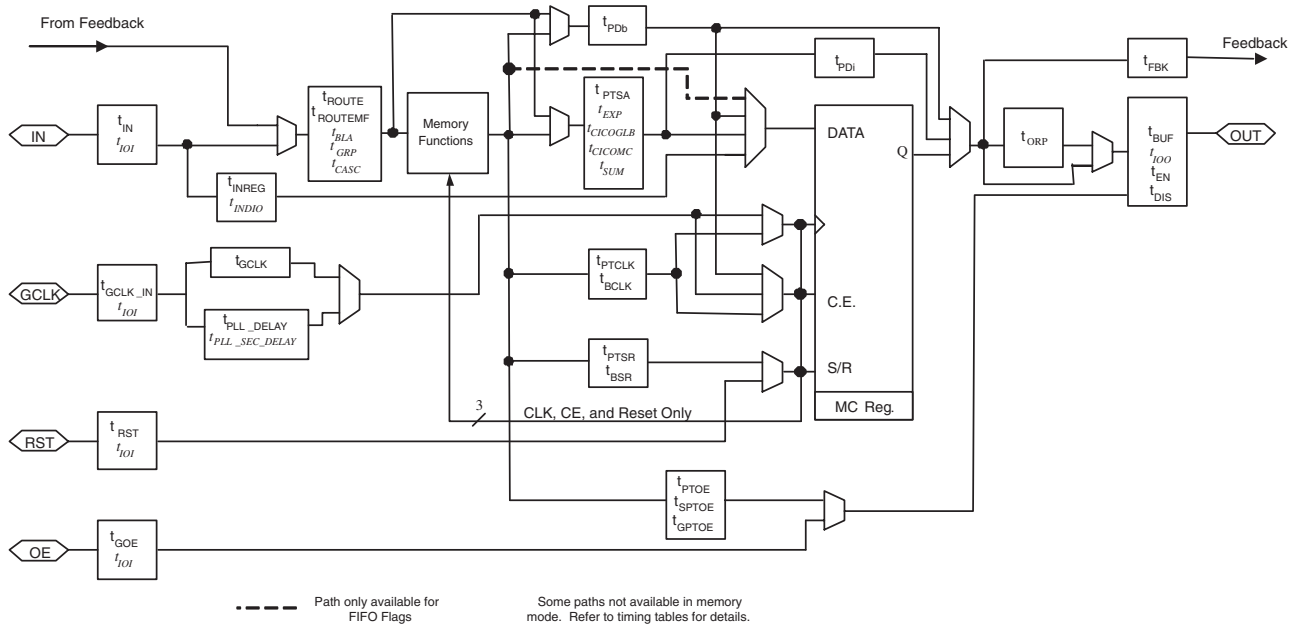
Parameter	Description	-4		-5		-75		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Data propagation delay, 5-PT bypass	—	4.0	—	5.0	—	7.5	—	10.0	ns
t_{PD_PTSA}	Data propagation delay	—	5.7	—	7.1	—	10.7	—	14.3	ns
t_S	GLB register setup time before clock, 5-PT bypass	2.9	—	3.6	—	5.4	—	7.3	—	ns
t_{S_PTSA}	GLB register setup time before clock	—	—	—	—	—	—	—	—	ns
t_{SIR}	GLB register setup time before clock, input register path	2.0	—	2.5	—	3.8	—	5.0	—	ns
t_H	GLB register hold time before clock, 5-Ptbypass	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{H_PTSA}	GLB register hold time before clock	—	—	—	—	—	—	—	—	ns
t_{HIR}	GLB register hold time before clock, input register path	0.0	—	0.0	—	0.0	—	0.0	—	ns
t_{CO}	GLB register clock-to-output delay	—	3.0	—	3.8	—	5.6	—	7.5	ns
t_R	External reset pin to output delay	—	4.5	—	5.6	—	8.4	—	11.3	ns
t_{RW}	Reset pulse duration	1.8	—	2.3	—	3.4	—	4.5	—	ns
$t_{LPTOE/DIS}$	Input to output local product term output enable/disable	—	6.0	—	7.5	—	11.3	—	15.0	ns
$t_{SPTOE/DIS}$	Input to output shared product term output enable/disable	—	6.0	—	7.5	—	11.3	—	15.0	ns
$t_{GOE/DIS}$	Global OE input to output enable/disable	—	4.2	—	5.3	—	7.9	—	10.5	ns
t_{CW}	Clock width, high or low	1.7	—	2.1	—	3.2	—	4.3	—	ns
t_{GW}	Gate width low (for low transparent) or high (for high transparent)	1.7	—	2.1	—	3.2	—	4.3	—	ns
t_{WIR}	Input register clock width, high or low	1.7	—	2.1	—	3.2	—	4.3	—	ns
t_{SKEW}	Clock-to-out skew, block level	—	0.6	—	0.8	—	1.1	—	1.5	ns
f_{MAX}[4]	Clock frequency with internal feedback	—	250	—	200	—	133	—	100	MHz
f_{MAX} (Ext.)	Clock frequency with external feedback, $1/ (t_{S\_PTSA} + t_{CO})$	—	—	—	—	—	—	—	—	MHz
f_{MAX} (Tog.)	Clock frequency max toggle	—	333	—	266	—	177	—	133	MHz
f_{MAX} (CAMC)	Clock frequency to CAM (configure mode)	—	—	—	—	—	—	—	—	MHz
f_{MAX} (CAM)	Clock frequency to CAM (compare mode)	—	—	—	—	—	—	—	—	MHz
f_{MAX} (RAM)	Clock frequency to RAM in - Single port Mode - Dual port Mode - Pseudo dual port Mode	—	—	—	—	—	—	—	—	MHz
t_{PWR_ON}	Power-on Time	—	—	—	—	—	—	—	—	uS

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other standards.
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using SRP feedback.

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing model show in Figure 18 shows the specific delay paths. Once the implementation of a given function is determined either conceptually of from the software report file, the delay path of a function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model. Note that internal timing parameters are for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

Figure 18. ispXPLD 5000MX Timing Model Diagram



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	0.5	—	ns
t_{PWL}	Input clock, low time	20 % to 20%	0.5	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 300	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	Output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 250	ps
		Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz and 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 100	ps
$T_{JIT(PERIOD)}$	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz	—	+/- 300	ps
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	500	ps
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)		+/- 170	+/- 480	ns
t_{RANGE}	Total output delay range (lead/lag)		+/- 1.19	+/- 3.36	ns
t_{PLL_RSTR}	Reset recovery time of the M-divider		—	—	ns
t_{PLL_RSTW}	Minimum reset pulse width		—	1.8	ns

1. This condition assures that the output phase jitter will remain within specification
2. Accumulated jitter measured over 10,000 waveform samples

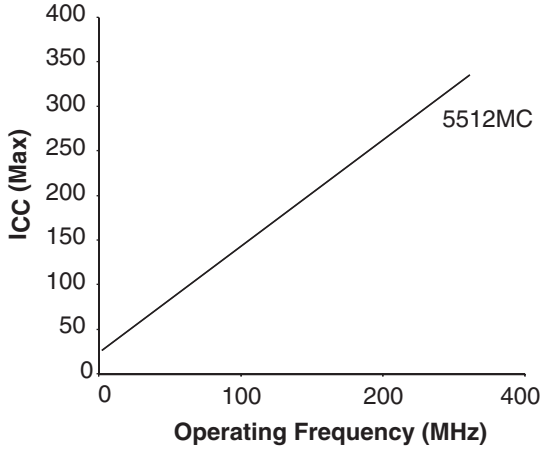
Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max	Units
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	8	—	ns
t_{BTH}	TCK [BSCAN] hold time	10	—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	10	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	ns

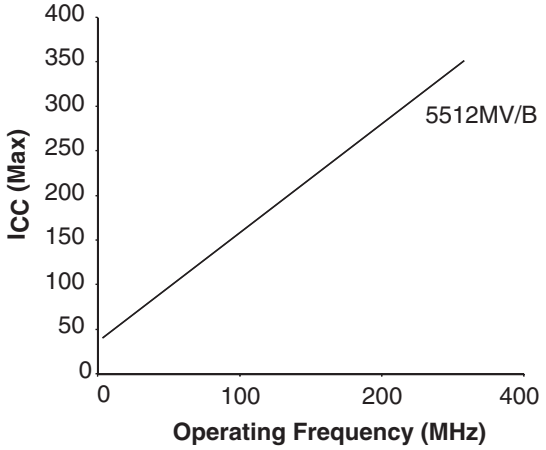
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 3.3V (MV) or 2.5V (MB), 25°C.

Power Estimation Coefficients

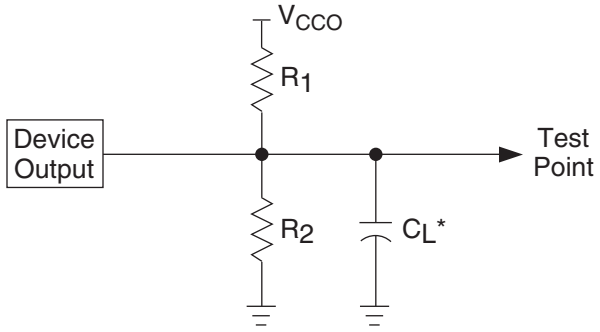
Device	K0	K1	K2	K3	K4	IDC	I_{DCO}	I_{PLL-DC}
ispXPLD 5000MC	--	--	--	--	--	--	--	--
ispXPLD 5000MB	--	--	--	--	--	--	--	--
ispXPLD 5000MV	--	--	--	--	--	--	--	--

K0 = Coefficient for power used when switching product terms
K1 = Coefficient for power used when switching routing
K2 = Coefficient for power used when switching memory
K3 = Coefficient for power used when switching a single PLL
IDC = Static logic current with no switching
IDCO = Static I/O bank current
IDC-PLL = Static current per PLL

Switching Test Conditions

Figure 19 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 12.

Figure 19. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 12. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CCO}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8V
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3.3 = 3.0V
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2.5 = 2.3V
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.8 = 1.65V
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65V
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65V
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65V

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the IEEE 1149.1 state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 state machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data out.
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the resisters in the device. The global polarity (active high or active low) for this pin is selectable on a global basis.
yzz	Input/Output – These are the general purpose I/O used by the logic array. *y* is the GLB reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs.
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GND	GND – Ground for PLLs.
V_{CCP}	V_{CC} - The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG interface.
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2CMOS or IEEE 1149.1 TAP.
$\overline{\text{PROGRAM}}$	Input – Controls the programming of SRAM. Hold high for normal operation. Toggle low to reload SRAM from E^2 memory.
CCLK	Input – Clock for sysCONFIG interface. Reads and writes occur on the rising edge of the clock.
READ	Input – Drive high to perform reads from the sysCONFIG interface.
$\overline{\text{INIT}}$	I/O – Indicates status of configuration. Can be driven low to inhibit configuration.
DONE	Output (open drain) – Indicates status of configuration.

ispXPLD 5512MX Power Supply and NC Connections[1]

Signals	208-Pin PQFP	256-Ball fpBGA	484-Ball fpBGA
V_{CC}	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4
V_{CCO0}	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4
V_{CCO1}	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3
V_{CCO2}	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20
V_{CCO3}	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19
V_{CCP}	136	J16	M22
V_{CCJ}	27	J1	M1
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8
GNDP	134	K16	N22
NC[2]	—	L1	AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	B4
0	109P	O28	O10	P16	O29	1	E4	A4
0	110N	O26	M17	O17	O27	2	B1	B3
0	110P	O24	M16	O16	O25	3	C1	A3
0	111N	O22	M15	O15	O23	4	D3	F5
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	V_{CCO0}
0	111P	O20	M14	O14	O21	6	C2	G6
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	GND (Bank 0)
0	112N	O18	M13	O13	O19	8	E3	H6
0	112P	O16	M12	O12	O17	9	D2	G5
0	113N	O14	O9	P14	O15	NC	NC	D3
0	113P	O12	O8	P12	O13	NC	NC	D2
0	114N	O10	O7	P10	O11	NC	NC	E4
0	114P	O8	O6	P8	O9	NC	NC	E3
0	115N	O6	O5	P6	O7	NC	NC	F4
0	115P	O4	O4	P4	O5	NC	NC	G4
0	116N	O2	O3	P2	O3	NC	NC	C2
—	—	V_{CCO0}	—	—	—	NC	V_{CCO0}	V_{CCO0}
0	116P	O0	O2	P0	O1	NC	NC	C1
—	—	GND (Bank 0)	—	—	—	NC	GND (Bank 0)	GND (Bank 0)
0	117N	P30	O1	—	P31	NC	D1	F3
0	117P	P28	O0	—	P29	NC	E1	G3
0	118N	P26	O31	—	P27	NC	F4	H4
—	—	V_{CC}	—	—	—	10	V_{CC}	V_{CC}
0	118P	P24	O30	—	P25	NC	F5	J4
0	119N	P22	M11	O11	P23	11	E2	H5
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	J5
0	120N	P18	M9	O9	P19	13	F1	E2
0	120P	P16	M8	O8	P17	14	G1	F2
—	—	GND	—	—	—	15	GND	GND
0	121N	P14	M7	O7	P15	16	F3	D1
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	V_{CCO0}
0	121P	P12	M6	O6	P13	18	G5	E1
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	GND (Bank 0)
0	122N	P10	M5	O5	P11	20	H5	J3
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	H2
0	123N	P6	—	—	P7	22	G3	G2
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	G1
0	124N	P2	—	—	P3	24	G2	H1
0	124P	P0	—	—	P1	25	H1	J1
—	—	GCLK0	—	—	—	26	H2	N7
—	—	V_{CCJ}	—	—	—	27	J1	M1
—	—	GCLK1	—	—	—	28	J2	P7

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	GND	—	—	—	29	K1	N1
—	—	TDI	—	—	—	30	H6	R1
—	—	TMS	—	—	—	31	H4	R2
—	—	TCK	—	—	—	32	J6	T1
—	—	TDO	—	—	—	33	K2	V1
1	0P	A0/DATA0	B0	D0	A1	34	K3	W1
1	0N	A2/DATA1	B1	D1	A3	35	J3	Y1
1	1P	A4/DATA2	B2	D2	A5	36	J5	P3
1	1N	A6/DATA3	B3	D3	A7	37	J4	R3
1	2P	A8/DATA4	B4	D4	A9	38	L2	T2
1	2N	A10/DATA5	B5	D5	A11	39	M1	U2
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	GND (Bank 1)
1	3P	A12/DATA6	B6	D6	A13	41	K4	V2
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	V_{CCO1}
1	3N	A14	B7	D7	A15	43	L3	W2
—	—	GND	—	—	—	44	GND	GND
1	4P	A16/INITB	B8	D8	A17	45	K5	R4
1	4N	A18/CSB	B9	D9	A19	46	L5	T4
1	5P	A20/READ	B10	D10	A21	47	N1	R6
1	5N	A22/CCLK	B11	D11	A23	48	M2	R5
1	6P	A24	—	—	A25	NC	NC	U3
—	—	VCC	—	—	—	49	VCC	VCC
1	6N	A26	—	—	A27	NC	P1	V3
1	7P	A28	—	—	A29	NC	M3	Y2
1	7N	A30	—	—	A31	NC	L4	W3
1	8P	B0	A0	—	B1	NC	N2	U5
1	8N	B2	A2	—	B3	NC	P2	T5
—	—	GND (Bank 1)	—	—	—	NC	GND (Bank 1)	GND (Bank 1)
1	9P	B4	A4	—	—	NC	R1	U4
—	—	V_{CCO1}	—	—	—	NC	V_{CCO1}	V_{CCO1}
1	9N	B5	A6	—	—	NC	R2	V4
1	10P	B6	A8	—	B7	NC	T2	AA3
1	10N	B8	A10	—	B9	NC	T3	AB3
1	—	B10	A12	—	B11	NC	NC	Y4
—	—	DONE	—	—	—	50	M4	AA4
1	11P	B14	B12	D12	B15	51	N3	AB4
1	11N	B16	B13	D13	B17	52	P4	AB5
1	12P	B18	B14	D14	B19	53	N5	T6
1	12N	B20	B15	D15	B21	54	M6	U7
—	—	PROGRAMB	—	—	—	55	R3	W5
1	—	B22	A14	—	B23	NC	P5	U8
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	GND (Bank 1)
1	13P	B24	A16	—	B25	NC	T4	V6

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	V_{CCO1}
1	13N	B26	A18	—	B27	NC	T5	V7
1	14P	B28	A20	—	B29	NC	R4	Y5
1	14N	B30	A22	—	B31	NC	N6	AA5
1	15P	C0	—	—	C1	NC	R5	Y6
1	15N	C2	—	—	C3	NC	P6	Y7
1	16P	C4	—	—	C5	NC	NC	AA6
1	16N	C8	—	—	C9	NC	NC	AA7
1	17P	C10	—	—	C11	NC	NC	W7
1	17N	C12	—	—	C13	NC	M7	V8
1	18P	C16	—	—	C17	NC	T6	W8
1	18N	C18	—	—	C19	NC	R6	U9
—	—	GND0 (Bank 1)	—	—	—	NC	GND (Bank 1)	GND (Bank 1)
—	—	CFG0	—	—	—	58	L8	U10
—	—	V_{CCO1}	—	—	—	NC	V_{CCO1}	V_{CCO1}
1	19P	C24	B16	D16	C25	59	T7	AB7
1	19N	C26	B17	D17	C27	60	R7	AA8
1	20P	C28	B18	D18	C29	61	N7	AB8
1	20N	D0	B19	D19	D1	62	P7	AB9
1	21P	D2	B20	D20	D3	63	T8	W9
1	21N	D4	B21	D21	D5	64	R8	Y9
1	22P	D6	B22	D22	D7	65	M8	AB10
1	22N	D8	B23	D23	D9	66	P8	AA10
1	—	D10/V_{REF1}	—	—	D11	67	L9	W10
1	23P	D12	B24	D24	D13	68	N8	Y10
1	23N	D16	B25	D25	D17	69	M9	Y11
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	GND (Bank 1)
1	24P	D18	B26	D26	D19	71	N10	V9
—	—	VCCO1	—	—	—	72	V_{CCO1}	V_{CCO1}
1	24N	D20	B27	D27	D21	73	T9	V10
1	25P	D22	B28	D28	D23	74	T10	AA11
1	25N	D24	B29	D29	D25	75	R9	AB11
—	—	VCC	—	—	—	76	VCC	VCC
1	26P	D26	B30	D30	D27	77	P9	U11
1	26N	D28	B31	D31	D29	78	N9	V11
2	27P	E0	F0	H0	E1	79	T11	AB12
2	27N	E2	F1	H1	E3	80	T12	AA12
—	—	GND	—	—	—	81	NC	GND
—	—	GND	—	—	—	NC	GND	GND
2	28P	E4	F2	H2	E5	82	P10	Y12
2	28N	E6	F3	H3	E7	83	R10	AA13
2	29P	E8	F4	H4	E9	84	R11	V12
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	V_{CCO2}

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
2	29N	E10	F5	H5	E11	86	M10	U12
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	GND (Bank 2)
2	30P	E12	F6	H6	E13	88	M11	AB13
2	30N	E16	F7	H7	E17	89	T13	Y13
2	31P	E18	—	—	E19	90	P11	V13
2	31N	E20/V_{REF2}	—	—	E21	91	T14	W13
2	32P	E22	F8	H8	E23	92	R12	V14
2	32N	E24	F9	H9	E25	93	R13	W14
2	33P	E26	F10	H10	E27	94	N11	Y14
2	33N	E28	F11	H11	E29	95	T15	AB14
2	34P	F0	F12	H12	F1	96	R14	AB15
2	34N	F2	F13	H13	F3	97	N12	AA15
2	35P	F4	F14	H14	F5	98	P12	U13
—	—	V_{CCO2}	—	—	—	NC	V_{CCO2}	V_{CCO2}
2	35N	F6	F15	H15	F7	99	R15	U14
—	—	GND (Bank 2)	—	—	—	NC	GND (Bank 2)	GND (Bank 2)
2	36P	F8	E0	—	F9	NC	NC	W15
2	36N	F10	E2	—	F11	NC	NC	W16
2	37P	F12	E4	—	F13	NC	NC	Y16
2	37N	F16	E6	—	F17	NC	NC	AA16
2	38P	F18	E8	—	F19	NC	NC	AB16
2	38N	F20	E10	—	F21	NC	NC	AA17
2	39P	F22	E12	—	F23	NC	NC	Y17
2	39N	F24	E16	—	F25	NC	NC	AA18
2	40P	F26	E20	—	F27	NC	NC	W17
2	40N	F28	E22	—	F29	NC	NC	W18
2	41P	G0	—	—	G1	NC	NC	V15
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	V_{CCO2}
2	41N	G2	—	—	G3	NC	NC	U15
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	GND (Bank 2)
2	42P	G4	—	—	G5	102	P13	Y18
2	42N	G6	—	—	G7	103	P15	V17
2	43P	G8	—	—	G9	NC	M13	V16
2	43N	G10	—	—	G11	NC	P14	U16
2	44P	G12	—	—	G13	NC	NC	AB18
2	44N	G14	—	—	G15	NC	NC	AB19
2	45P	G16	—	—	G17	NC	NC	U18
2	45N	G18	—	—	G19	NC	NC	T17
2	46P	G20	—	—	G21	104	R16	AB20
2	46N	G22	—	—	G23	105	P16	AA20
2	47P	G24	—	—	G25	106	N15	Y19
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	V_{CCO2}
2	47N	G26	—	—	G27	108	N14	V19

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	GND (Bank 2)
2	48P	G28	F16	H16	G29	110	N16	T18
2	48N	G30	F17	H17	G31	111	M16	R17
2	49P	H0	F18	H18	H1	112	M14	U19
2	49N	H2	F19	H19	H3	113	M15	T19
2	50P	H4	E24	—	H5	NC	NC	V20
—	—	V_{CC}	—	—	—	114	VCC	VCC
2	50N	H6	E26	—	H7	NC	NC	U20
2	51P	H8	F20	H20	H9	115	L13	W20
2	51N	H10	F21	H21	H11	116	L12	Y21
2	52P	H12	F22	H22	H13	117	L15	R18
2	52N	H14	F23	H23	H15	118	L16	R19
—	—	GND	—	—	—	119	GND	GND
2	53P	H16	F24	H24	H17	120	L14	W21
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	V_{CCO2}
2	53N	H18	F25	H25	H19	122	K15	Y22
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	GND (Bank 2)
2	54P	H20	F26	H26	H21	124	K14	R20
2	54N	H22	F27	H27	H23	125	K12	P20
2	55P	H24	F28	H28	H25	126	K13	T21
2	55N	H26	F29	H29	H27	127	J13	R21
2	56P	H28	F30	H30	H29	128	J14	U21
2	56N	H30	F31	H31	H31	129	J12	V21
—	—	TOE	—	—	—	130	J15	W22
—	—	RESET	—	—	—	131	J11	V22
—	—	GOE0	—	—	—	132	H11	T22
—	—	GOE1	—	—	—	133	H13	R22
—	—	GNDP	—	—	—	134	K16	N22
—	—	GCLK2	—	—	—	135	H15	P16
—	—	V_{CCP}	—	—	—	136	J16	M22
—	—	GCLK3	—	—	—	137	H16	N16
3	57N	I30	—	—	I31	138	H14	J22
3	57P	I28	—	—	I29	139	G16	H22
3	58N	I26	—	—	I27	140	G15	E22
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	E21
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	G22
3	59P	I20	I26	K26	I21	143	G14	F21
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	GND (Bank 3)
3	60N	I18	I25	K25	I19	145	F16	H21
—	—	VCCO3	—	—	—	146	V_{CCO3}	V_{CCO3}
3	60P	I16	I24	K24	I17	147	E16	G21
—	—	GND	—	—	—	148	GND	GND
3	61N	I14	I23	K23	I15	149	G13	D22

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
3	61P	I12	I22	K22	I13	150	G12	D21
3	62N	I10	I21	K21	I11	151	F14	J20
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	J19
3	63N	I6	K31	—	I7	NC	F12	E20
—	—	V_{CC}	—	—	—	153	VCC	VCC
3	63P	I4	K30	L30	I5	NC	F13	F20
3	64N	I2	K29	L28	I3	NC	D16	H17
3	64P	I0	K28	L26	I1	NC	D15	H18
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	65N	J30	K27	—	J31	NC	NC	J18
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	65P	J28	K26	—	J29	NC	NC	H19
3	66N	J26	K25	—	J27	NC	NC	G20
3	66P	J24	K24	—	J25	NC	NC	G19
3	67N	J22	K23	—	J23	NC	NC	C22
3	67P	J20	K22	—	J21	NC	NC	C21
3	68N	J18	K21	—	J19	NC	NC	D20
3	68P	J16	K20	—	J17	NC	NC	C19
3	69N	J14	K19	—	J15	NC	C16	F19
3	69P	J12	K18	—	J13	NC	B16	E19
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	70N	J10	K17	—	J11	NC	C15	G18
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	70P	J8	K16	—	J9	NC	B15	F18
3	71N	J6	K15	—	J7	NC	E14	B20
3	71P	J4	K14	—	J5	NC	D14	B19
3	72N	J2	K13	—	J3	NC	E13	A20
3	72P	J0	K12	—	J1	NC	A15	A19
3	73N	K30	I19	K19	K31	154	D12	D18
3	73P	K28	I18	K18	K29	155	B14	C18
3	74N	K26	I17	K17	K27	156	C13	G17
3	74P	K24	I16	K16	K25	157	A14	F16
3	75N	K22	I31	K31	K23	158	A13	E17
3	75P	K21	I30	K30	K22	159	B13	D17
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	GND (Bank 3)
3	76N	K20	K11	L21	K21	NC	D11	B18
—	—	V_{CCO3}	—	—	—	161	V_{CCO3}	V_{CCO3}
3	76P	K18	K10	L20	K19	NC	B12	A18
3	77N	K16	K9	L18	K17	NC	C12	C17
3	77P	K14	K8	L16	K15	NC	E11	B17
3	78N	K12	K7	L12	K13	NC	NC	C16
3	78P	K10	K6	L10	K11	NC	NC	B16
3	79N	K8	K5	L8	K9	NC	NC	F13

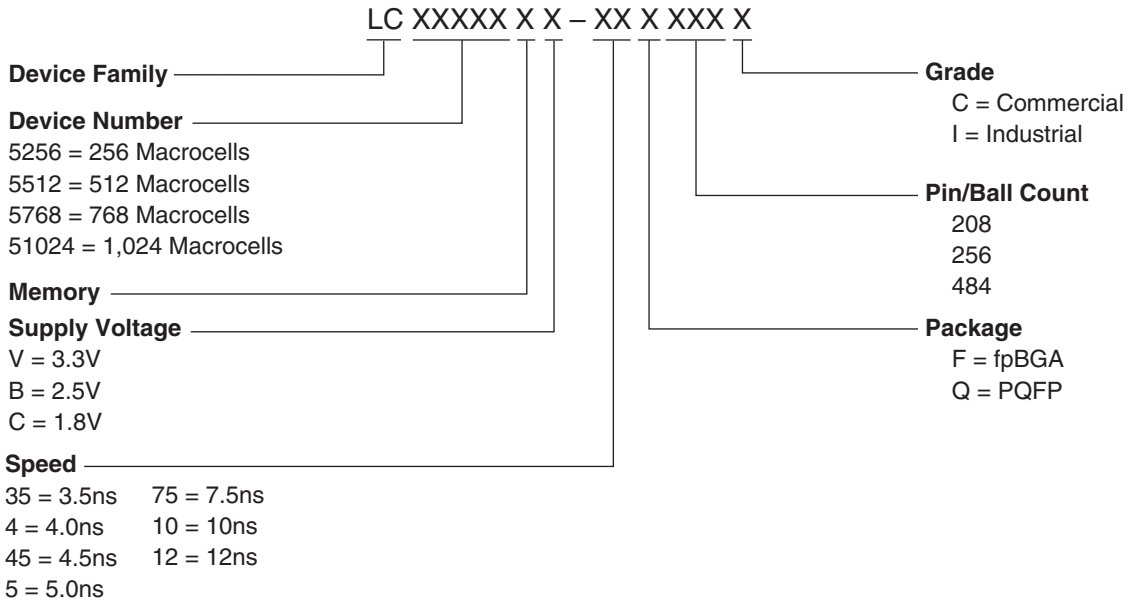
ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
3	79P	K6	K4	L6	K7	NC	NC	F15
3	80N	K5	K3	L5	—	NC	NC	D16
3	80P	K4	K2	L4	—	NC	E10	E16
3	81N	K2	K1	L2	K3	NC	A12	A16
3	81P	K0	K0	L0	K1	NC	A11	A15
—	—	GND (Bank 3)	—	—	—	NC	GND (Bank 3)	GND (Bank 3)
3	82N	L30	I15	K15	L31	162	B11	B15
—	—	V_{CCO3}	—	—	—	NC	V_{CCO3}	V_{CCO3}
3	82P	L28	I14	K14	L29	163	C11	A14
3	83N	L26	I13	K13	L27	164	B10	D15
3	83P	L24	I12	K12	L25	165	A10	E15
3	84N	L22	I11	K11	L23	166	C10	D14
3	84P	L21	I10	K10	L22	167	D10	F14
3	85N	L20	I9	K9	L21	168	C9	A13
3	85P	L18	I8	K8	L19	169	E9	B13
3	86N	L16/VREF3	I29	K29	L17	170	D9	C14
3	86P	L14	I28	K28	L15	171	F9	E14
3	87N	L12	I7	K7	L13	172	A9	E13
3	87P	L10	I6	K6	L11	173	F8	F12
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	GND (Bank 3)
3	88N	L8	I5	K5	L9	175	E8	D13
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	V_{CCO3}
3	88P	L6	I4	K4	L7	177	A8	C13
3	89N	L5	I3	K3	—	178	B9	E12
3	89P	L4	I2	K2	—	179	D8	C12
—	—	VCC	—	—	—	180	L11	VCC
3	90N	L2	I1	K1	L3	181	B8	B12
3	90P	L0	I0	K0	L1	182	C8	A12
0	91N	M30	M31	O31	M31	183	B7	E11
0	91P	M28	M30	O30	M29	184	A7	C11
—	—	GND	—	—	—	185	NC	GND
—	—	GND	—	—	—	NC	GND	GND
0	92N	M26	M29	O29	M27	186	D7	B11
0	92P	M24	M28	O28	M25	187	C7	A11
0	93N	M22	M27	O27	M23	188	B6	F11
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	V_{CCO0}
0	93P	M21	M26	O26	M22	190	E7	F10
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	GND (Bank 0)
0	94N	M20	M25	O25	M21	192	E6	E10
0	94P	M18	M24	O24	M19	193	A6	C10
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	D10
0	95P	M14	M2	O2	M15	195	A4	B10
0	96N	M12	M23	O23	M13	196	B5	A10

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Pin Number	484 fpBGA Pin Number
			Macrocell 1	Macrocell 2				
0	96P	M10	M22	O22	M11	197	A3	A9
0	97N	M8	M21	O21	M9	198	B4	C9
0	97P	M6	M20	O20	M7	199	B3	D9
0	98N	M5	M19	O19	—	200	C5	F9
0	98P	M4	M18	O18	—	201	C6	E9
0	99N	M2	M1	O1	M3	202	D5	A8
—	—	V_{CCO0}	—	—	—	NC	V_{CCO0}	V_{CCO0}
0	99P	M0	M0	O0	M1	203	D6	B8
—	—	GND (Bank 0)	—	—	—	NC	GND (Bank 0)	GND (Bank 0)
0	100N	N30	O29	—	N31	NC	NC	A7
0	100P	N28	O28	—	N29	NC	NC	B7
0	101N	N26	O27	—	N27	NC	NC	A5
0	101P	N24	O26	—	N25	NC	NC	B5
0	102N	N22	O25	—	N23	NC	NC	B6
0	102P	N21	O24	—	N22	NC	NC	C7
0	103N	N20	O23	—	N21	NC	NC	E8
0	103P	N18	O22	—	N19	NC	NC	E7
0	104N	N16	O21	—	N17	NC	NC	E6
0	104P	N14	O20	—	N15	NC	NC	D6
0	105N	N12	O19	—	N13	NC	NC	D8
—	—	V_{CCO0}	—	—	—	204	V_{CCO0}	V_{CCO0}
0	105P	N10	O18	—	N11	NC	NC	F8
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	GND (Bank 0)
0	106N	N8	O17	—	N9	NC	NC	F7
0	106P	N6	O16	—	N7	NC	NC	D7
0	107N	N5	O15	—	—	206	A2	C6
0	107P	N4	O14	—	—	207	B2	C5
0	108N	N2	O13	—	N3	NC	NC	C4
0	108P	N0	O12	—	N1	NC	NC	D5

Part Number Description



Ordering Information

Commercial

Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count
LC5512MV-4Q208C	512	3.3	4.0	PQFP	208
LC5512MV-5Q208C	512	3.3	5.0	PQFP	208
LC5512MV-75Q208C	512	3.3	7.5	PQFP	208
LC5512MV-4F256C	512	3.3	4.0	fpBGA	256
LC5512MV-5F256C	512	3.3	5.0	fpBGA	256
LC5512MV-75F256C	512	3.3	7.5	fpBGA	256
LC5512MV-4F484C	512	3.3	4.0	fpBGA	484
LC5512MV-5F484C	512	3.3	5.0	fpBGA	484
LC5512MV-75F484C	512	3.3	7.5	fpBGA	484
LC5512MB-4Q208C	512	2.5	4.0	PQFP	208
LC5512MB-5Q208C	512	2.5	5.0	PQFP	208
LC5512MB-75Q208C	512	2.5	7.5	PQFP	208
LC5512MB-4F256C	512	2.5	4.0	fpBGA	256
LC5512MB-5F256C	512	2.5	5.0	fpBGA	256
LC5512MB-75F256C	512	2.5	7.5	fpBGA	256
LC5512MB-4F484C	512	2.5	4.0	fpBGA	484
LC5512MB-5F484C	512	2.5	5.0	fpBGA	484
LC5512MB-75F484C	512	2.5	7.5	fpBGA	484
LC5512MC-4Q208C	512	1.8	4.0	PQFP	208
LC5512MC-5Q208C	512	1.8	5.0	PQFP	208
LC5512MC-75Q208C	512	1.8	7.5	PQFP	208
LC5512MC-4F256C	512	1.8	4.0	fpBGA	256
LC5512MC-5F256C	512	1.8	5.0	fpBGA	256

Commercial (Continued)

Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count
LC5512MC-75F256C	512	1.8	7.5	fpBGA	256
LC5512MC-4F484C	512	1.8	4.0	fpBGA	484
LC5512MC-5F484C	512	1.8	5.0	fpBGA	484
LC5512MC-75F484C	512	1.8	7.5	fpBGA	484

Industrial

Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count
LC5512MV-5Q208I	512	3.3	5.0	PQFP	208
LC5512MV-75Q208I	512	3.3	7.5	PQFP	208
LC5512MV-10Q208I	512	3.3	10.0	PQFP	208
LC5512MV-5F256I	512	3.3	5.0	fpBGA	256
LC5512MV-75F256I	512	3.3	7.5	fpBGA	256
LC5512MV-10F256I	512	3.3	10.0	fpBGA	256
LC5512MV-5F484I	512	3.3	5.0	fpBGA	484
LC5512MV-75F484I	512	3.3	7.5	fpBGA	484
LC5512MV-10F484I	512	3.3	10.0	fpBGA	484
LC5512MB-5Q208I	512	2.5	5.0	PQFP	208
LC5512MB-75Q208I	512	2.5	7.5	PQFP	208
LC5512MB-10Q208I	512	2.5	10.0	PQFP	208
LC5512MB-5F256I	512	2.5	5.0	fpBGA	256
LC5512MB-75F256I	512	2.5	7.5	fpBGA	256
LC5512MB-10F256I	512	2.5	10.0	fpBGA	256
LC5512MB-5F484I	512	2.5	5.0	fpBGA	484
LC5512MB-75F484I	512	2.5	7.5	fpBGA	484
LC5512MB-10F484I	512	2.5	10.0	fpBGA	484
LC5512MC-5Q208I	512	1.8	5.0	PQFP	208
LC5512MC-75Q208I	512	1.8	7.5	PQFP	208
LC5512MC-10Q208I	512	1.8	10.0	PQFP	208
LC5512MC-5F256I	512	1.8	5.0	fpBGA	256
LC5512MC-75F256I	512	1.8	7.5	fpBGA	256
LC5512MC-10F256I	512	1.8	10.0	fpBGA	256
LC5512MC-5F484I	512	1.8	5.0	fpBGA	484
LC5512MC-75F484I	512	1.8	7.5	fpBGA	484
LC5512MC-10F484I	512	1.8	10.0	fpBGA	484

Note: The speed grades on these devices are dual marked. For example, the commercial speed grade –4XXXXC is also marked with the industrial grade –5XXXXI. The commercial grade is always one speed grade faster than the associated dual mark industrial grade.

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispXPLD 5000MX family:

- sysIO Design and Usage Guidelines for Lattice Devices (TN1000)
- sysCLOCK PLL Design and Usage Guidelines (TN1003)
- Power Estimation in ispXPLD 5000MX Devices (TN1031)
- Using Memory in ispXPLD 5000MX Devices (TN1030)
- sysCONFIG Interface Usage Guidelines (TN1026)